Please amend the subject application as follows:

IN THE CLAIMS:

1. (Original) An integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:
   a first substrate trace having a first end and a second end;
   a second substrate trace having a first end, said second substrate trace being laterally aligned with said first substrate trace;
   a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said second substrate trace using a first wire;
   a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said first substrate trace using a second wire; and
   a third substrate trace having a first end, said first end of said third substrate trace coupled to said second end of said first substrate trace using a third wire, wherein said third wire crosses over said second substrate trace.

2. (Original) The integrated circuit of claim 1 wherein said third wire crosses over said second substrate trace at a location approximately midway between a first end and a second end of said third wire and approximately midway between said first end and a second end of said second substrate trace.

3. (Original) The integrated circuit of claim 1 wherein the first substrate trace and the third substrate trace have approximately equal surface area.

4. (Original) The integrated circuit of claim 1 wherein at least one aggressor signal generates an interfering magnetic field, said interfering magnetic field generating a first magnetic flux between said first substrate trace and said second substrate trace, said interfering magnetic field generating a second magnetic flux between said second substrate trace and said third substrate trace, said first magnetic flux canceling out a substantial portion of said second magnetic flux.

5. (Original) The integrated circuit of claim 1, wherein at least one of said first substrate trace, said second substrate trace, and said third substrate trace are made of copper or tungsten.

Claims 6-20 (Canceled)

21. (New) A method of forming an integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:

providing a first substrate trace having a first end and a second end;

providing a second substrate trace having a first end, said second substrate trace being laterally aligned with said first substrate trace;

providing a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said second substrate trace using a first wire;

providing a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said first substrate trace using a second wire; and

providing a third substrate trace having a first end, said first end of said third substrate trace coupled to said second end of said first substrate trace using a third wire, wherein said third wire crosses over said second substrate trace.

22. (New) The method of claim 21 further comprising crossing the third wire over said second substrate trace at a location approximately midway between a first end and a second end of said third wire and approximately midway between said first end and a second end of said second substrate trace.

23. (New) The method of claim 21 further comprising providing the first substrate trace and the third substrate trace with approximately equal surface area.

24. (New) The method of claim 21 further comprising generating an interfering magnetic field with at least one aggressor signal, said interfering magnetic field generating a first magnetic flux between said first substrate trace and said second substrate trace, said interfering magnetic field generating a second magnetic flux between said second substrate trace and said third substrate trace, said first magnetic flux canceling out a substantial portion of said second magnetic flux.

25. (New) The method of claim 21 further comprising forming at least one of said first substrate trace, said second substrate trace or said third substrate trace with copper or tungsten.

26. (New) An integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:

a first substrate trace comprising a first end and a second end;

a second substrate trace comprising a first end, said second substrate trace being parallel to said first substrate trace and farther from the semiconductor die than the first substrate trace;

a third substrate trace comprising a first portion thereof positioned between the first substrate trace and the second substrate, the third substrate trace comprising a second portion thereof positioned lateral to and in parallel with the first substrate trace, the third substrate trace comprising a third portion thereof positioned lateral to and in parallel with the second substrate trace;

a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said first substrate trace using a first wire;

a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said third substrate trace using a second wire; and

a third wire for coupling said second end of said first substrate trace to said first end of said second substrate trace, wherein said third wire crosses over said first portion of said third substrate trace.

27. (New) The integrated circuit of claim 26 wherein one of the first wire or the second wire crosses over the other.

28. (New) The integrated circuit of claim 26 wherein the second substrate trace and the third substrate trace terminate at a respective first via and second via.

29. (New) The integrated circuit of claim 26 wherein the first substrate trace and the second substrate trace have approximately equal surface area.

30. (New) The integrated circuit of claim 26 wherein said third wire crosses over said third substrate trace at a location approximately midway between a first end and a second end of said third wire and approximately midway between said first end and a second end of said second substrate trace.

31. (New) The integrated circuit of claim 26 wherein the second portion and the third portion of the third substrate trace have a substantially same length.